

1 METHOD AND CIRCUIT ARRANGEMENT FOR MONITORING THE MODE OF
2 OPERATION OF ONE OR MORE LOAD CIRCUITS, ESPECIALLY OF A
3 DOMESTIC APPLIANCE
4

5 The invention relates to a method and a circuit arrangement for monitoring the
6 mode of operation of one or more load circuits, especially of a domestic
7 appliance, which comprises a controlled semiconductor switch, especially a triac,
8 and an electric consumer connected thereto, which are supplied by at least one
9 alternating voltage source, that supplies an alternating voltage including positive
10 and negative voltage half-waves.

11
12 For monitoring the mode of operation of a load circuit containing a dc motor it is
13 already known (see for example, Siemens switching examples, 1982/83 edition,
14 page 37, Fig. 2.2 and page 47, Fig. 2.5) to pass the current flowing in the load
15 circuit via a low-impedance precision resistor (shunt resistor) and evaluate the
16 voltage drop at this precision resistor by means of an operational amplifier.
17 Monitoring the mode of operation of one or more load circuits supplied by at least
18 one alternating voltage source, that is not supplied by a dc voltage, is not known
19 in this connection.

20
21 It is thus the object of the invention to show a way of monitoring the mode of
22 operation of one or more load circuits supplied by at least one alternating voltage
23 source, in a relatively simple manner.

24
25 The object indicated previously is solved according to the invention in a method of
26 the type specified initially by guiding the currents flowing through all controlled
27 semiconductor switches and electric consumers through a common low-
28 impedance precision resistor and separately evaluating the respective voltage
29 drop occurring at this low-impedance precision resistor with regard to the
30 amplitudes of the positive and negative voltage half-waves.

31
32 The present invention uses a low-impedance precision resistor as in the prior art
33 considered above but in this case, only a single low-voltage precision resistor is
34 provided for all the existing load circuits. In addition, in the present invention the
35 respective positive and negative voltage drops occurring separately at the single
36 low-voltage precision resistor used, which are attributable to the current flows
37 through all the monitored load circuits, are evaluated separately. As a result, if
38 one or more of the load circuits is working incorrectly, conclusions on various

1 faults in the load circuits concerned can be drawn according to whether, and
2 optionally which, of the positive and/or negative voltage drops at said single low-
3 voltage precision resistor are equal to predefined rated values. For example, from
4 a rise in the positive and the negative voltage drops at said single precision
5 resistor above predefined rated values in the case of an electric motor
6 representing an electrical consumer, such as a pump motor of a domestic
7 appliance, it can be deduced that this motor is not running correctly. In the case
8 of a positive or negative voltage drop at said single low-impedance precision
9 resistor which deviates from a predefined rated value, a faulty operating mode of
10 one or more controlled semiconductor switches can be recognised for example.
11 This leads to a limitation of possible faulty parts of the monitored load circuits.

12

13 Preferably used for carrying out the method according to the invention is a circuit
14 arrangement which is characterised in that all the electric consumers together with
15 their relevant controlled semiconductor switches are connected via a low-
16 impedance precision resistor to the at least one alternating voltage source and
17 that an evaluation arrangement which evaluates the positive and the negative
18 voltage half-waves of said alternating voltage is connected to said low-impedance
19 precision resistor. This yields the advantage of a particularly low expenditure on
20 circuitry to monitor the mode of operation of one or more load circuits according to
21 the invention.

22

23 More appropriately, the evaluating arrangement comprises a first evaluating
24 device which evaluates the positive voltage half-waves of the relevant alternating
25 voltage and a second evaluating device which evaluates the negative voltage half-
26 waves of the relevant alternating voltage. The advantage of an evaluating device
27 having a particularly simple structure is hereby obtained.

28 A particularly low expenditure on circuitry is advantageously obtained if each of
29 the two evaluating devices is formed by an operational amplifier which has its
30 inverting input and its non-inverting input connected to the two ends of said low-
31 impedance precision resistor.

32 More appropriately in this case, a first operational amplifier has its non-inverting
33 input and a second operational amplifier has its inverting input connected to one
34 end of said precision resistor and said first operational amplifier has its inverting
35 input and said second operational amplifier has its non-inverting input connected
36 to the other end of said precision resistor. As a result of this circuitry measure, the
37 two said operational amplifiers can evaluate different-priority voltage half-waves of
38 the respective decreasing alternating voltage at said precision resistor.

1
2 According to another appropriate embodiment of the present invention, connected
3 to the outputs of the two operational amplifiers is an evaluating circuit which
4 compares the output signals respectively delivered by the two operational
5 amplifiers with specified threshold voltages and which, depending on the
6 magnitudes by which the output voltages respectively delivered by the relevant
7 operational amplifiers exceed or fall below said specified threshold voltages,
8 delivers status signals which either indicate a correct current flow or a perturbed
9 current flow through the respective electric consumers and the controlled
10 semiconductor switches associated therewith. This yields the advantage of a
11 particularly low expenditure on circuitry for the construction of said evaluating
12 circuit; in principle, this evaluating circuit can manage with two voltage
13 comparators.

14
15 The method and the circuit arrangement according to the invention are explained
16 in detail with reference to a drawing.

17 The drawing shows an exemplary embodiment of a circuit arrangement according
18 to the present invention. The relevant circuit arrangement is used in the present
19 case for monitoring the operating mode of two load circuits which especially can
20 be provided in a domestic appliance such as a washing machine, a dishwasher, a
21 drier etc. Of the two load circuits shown, one comprises an electric consumer R1
22 and the other comprises an electric consumer R2. These electric consumers R1,
23 R2 can, for example, be electric motors or heating resistors. The two electric
24 consumers shown R1 and R2 are each connected in series with a controlled
25 semiconductor switch T1 or T2 and specifically with the load section of the
26 respective semiconductor switch T1 or T2. In the present case, the relevant
27 controlled semiconductor switches are formed by triacs whose control electrodes
28 are connected to control outputs of a control circuit Ctr, not described in detail,
29 which are supplied by an alternating voltage source Vac indicated in the drawing.
30 Instead of the aforementioned triacs, however, other controlled semiconductor
31 switches can also be used such as thyristors, power transistors such as so-called
32 power MOSFETS etc.

33
34 All the controlled semiconductor switches T1, T2 provided and the electric
35 consumers R1 or R2 connected thereto are jointly connected via a low-impedance
36 precision resistor Rm to an alternating voltage source Vac which supplies an
37 alternating voltage comprising positive and negative voltage half-waves and
38 which, for example, can be the usual mains alternating voltage of 230 V, 50 Hz.

1
2 However, it is possible in principle to provide each of the consumer circuits
3 provided with its own alternating voltage source.
4

5 An evaluating arrangement Ed which separately evaluates the positive and the
6 negative half-waves of the decreasing alternating voltage at this precision resistor
7 is connected to the low-impedance precision resistor Rm whose resistance
8 depends on the magnitude of the maximum predicted flowing currents and which
9 can have a value of 0.1 Ohm for example. This evaluating arrangement Ed
10 comprises two evaluating devices in the form of respectively one operational
11 amplifier Op1, Op2.
12

13 The operational amplifier Op1 to be designated as first operational amplifier has
14 its non-inverting input (+) connected to the common connection point of the triac
15 T1, T2 and the low-impedance precision resistor Rm and has its inverting input (-)
16 connected via a resistor R5 to the other end of the precision resistor Rm. The
17 output of the first operational amplifier Op1 is further connected via the resistor R3
18 to this other end of the precision resistor Rm which can optionally be earthed or
19 be at earth potential. The relevant output of the first operational amplifier Op1 is
20 also connected via a resistor R4 to its inverting input (-).
21

22 The operational amplifier Op2 to be designated as the second operational
23 amplifier, which furthermore can be or is of the same type of operational amplifier
24 as the first operational amplifier Op1, has its inverting input (-) connected via a
25 resistor R8 to the common connection point of the triac T1, T2 and the low-
26 impedance precision resistor Rm. The non-inverting input (+) of the second
27 operational amplifier Op2 is connected to the other end of the low-impedance
28 precision resistor Rm. The output of the second operational amplifier Op2 is firstly
29 connected via a resistor R6 to the common connection point of the triac T1, T2
30 and the low-impedance precision resistor Rm and secondly it is connected via a
31 resistor R7 to its inverting input (-).
32

33 With respect to the two operational amplifiers Op1, Op2 considered previously, it
34 should also be noted that the supply voltage sources required for these
35 operational amplifiers and their connection to the relevant operational amplifiers
36 are not shown here since this has nothing to do with the present invention as
37 such.
38

1 As a result of the previously explained type of connection of the two operational
2 amplifiers Op1, Op2 with their non-inverting inputs (+) and inverting inputs (-) to
3 the low-impedance precision resistor Rm, it is found that the first operational
4 amplifier Op1 operates as a non-inverting amplifier and evaluates the positive
5 half-waves of the respectively decreasing voltage at the low-impedance precision
6 resistor Rm. In contrast, the second operational amplifier Op2 operates as an
7 inverting amplifier which evaluates the negative half-waves of the respectively
8 decreasing voltage at the low-impedance precision resistor Rm.

9
10 The output signals respectively delivered in this manner from the outputs of the
11 two operational amplifiers Op1, Op2 are supplied in the case of the first
12 operational amplifier Op1 to the input I1 of an evaluating circuit Ec and in the case
13 of the second operational amplifier Op2 to the input I2 of the relevant evaluating
14 circuit Ec. This evaluating circuit compares the relevant output signals with
15 specified threshold voltages and depending on the magnitude by which the output
16 signals respectively delivered by said operational amplifiers Op1, Op2 exceed or
17 fall below specified threshold voltages, delivers status signals to outputs O1 or O2
18 which either indicate a correct current flow or a perturbed current flow through the
19 respective load circuit, comprising in the present case on the one hand the electric
20 consumer R1 and the triac T1 in series therewith and on the other hand, the
21 electric consumer R2 and the triac T2 in series therewith with its main load
22 section.

23
24 In the operating mode of the load circuits shown in the drawing which has been
25 considered previously, it has been assumed that these are all operating
26 simultaneously. In this case, a status signal indicating a perturbed current flow
27 which appears at one of the outputs O1, O2, for example, with a high level
28 indicates that there is a fault in at least one of the relevant load circuits. In this
29 case, the aforementioned threshold voltages are stipulated according to the
30 overall operation of all the load circuits. A status signal which appears with a low
31 level for example would then indicate correct operation of the detected load
32 circuits.

33
34 In principle, however, it is also possible for all the existing load circuits to be
35 divided into groups each comprising a plurality of load circuits and for the load
36 circuits belonging to respectively one such load circuit group to be operated at the
37 same time. In this case, threshold voltages corresponding to the normal current
38 values of the respective load circuit group would then need to be provided in the

1 evaluation circuit Ec. That is, a corresponding synchronisation must be produced
2 between the delivery of control signals by the control device Ctr and the provision
3 of the respectively relevant threshold voltages in the evaluation circuit Ec. This
4 synchronisation can be achieved, for example, by a synchronous switch-over in
5 the control signal delivery and the provision of the threshold voltage.

6
7 In order to ascertain which individual load circuit is operating incorrectly, the
8 aforesaid synchronisation between the delivery of the control signals by the
9 control device Ctr and the provision of the respectively relevant threshold voltage
10 in the evaluation circuit Ec should be extended to each individual load circuit. For
11 this purpose, firstly the controlled semiconductor switches of the existing load
12 circuits are individually activated one after the other and secondly, individually
13 relevant threshold voltages are provided for the load circuits concerned in the
14 evaluation circuit Ec. The status signals thereby determined are then individually
15 assigned to the relevant load circuits whereby the fault can rapidly be isolated.

16
17 As a result of the afore-mentioned status signals, in the event that an electric
18 consumer is formed by a circulating pump without separate speed feedback, a
19 too-high current flow relative to a predetermined rated value can be identified and
20 it can be deduced therefrom that the relevant circulating pump is blocked
21 whereupon the circuit of the relevant circulating pump can be immediately shut
22 down. This means that the controlled semiconductor switches in the load circuit of
23 this electric consumer can have a lower power and smaller cooling area than in
24 the case where such a shutdown cannot take place immediately because of a lack
25 of corresponding monitoring.

26
27 In addition, the monitoring of the mode of operation of the respectively provided
28 load circuits undertaken by the evaluation arrangement Ed described can be
29 represented by a plain-text display or by a seven-segment display by means of
30 corresponding display devices which can result in simplified and more rapid fault
31 finding when the mode of operation of the relevant load circuits is disturbed. In
32 this connection, it can also be displayed that no fault is detected or that the load
33 circuits are operating correctly. These types of displays could also be made
34 available to customer service by remote interrogation to be able to make
35 diagnoses beforehand. In this case, the present invention makes fault finding
36 simpler and more rapid in the event of faulty operation of one or more load
37 circuits.

38

1 In addition, a permanent mode (full-wave mode) and a half-wave mode in the
2 respective load circuit can be easily identified by the present invention. The
3 identification of a continuous half-wave mode especially when using pump motors
4 as electric consumers is especially important since these pump motors are
5 destroyed during continuous half-wave operation. Remedial measures are
6 provided here by full-wave control of the relevant motors associated with the
7 output of a corresponding warning and shutdown of the relevant pump motors
8 which is initially possible. This can be ensured by the present invention.

9
10 Finally, it should be noted that the present invention has been explained
11 previously in connection with monitoring of the operating mode of two load
12 circuits. However, the invention is not restricted thereto; rather, it can be used for
13 monitoring the mode of operation of at least one load circuit but also for
14 monitoring the mode of operation of more than two load circuits.

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